

Amendments to the Drawings:

The attached sheets of drawings include changes to Figures 4-9 to add the designation --Prior Art--. These sheets, which include Figs. 4-9, replace the original sheets including Figs. 4-9.

Attachments: Replacement Sheets

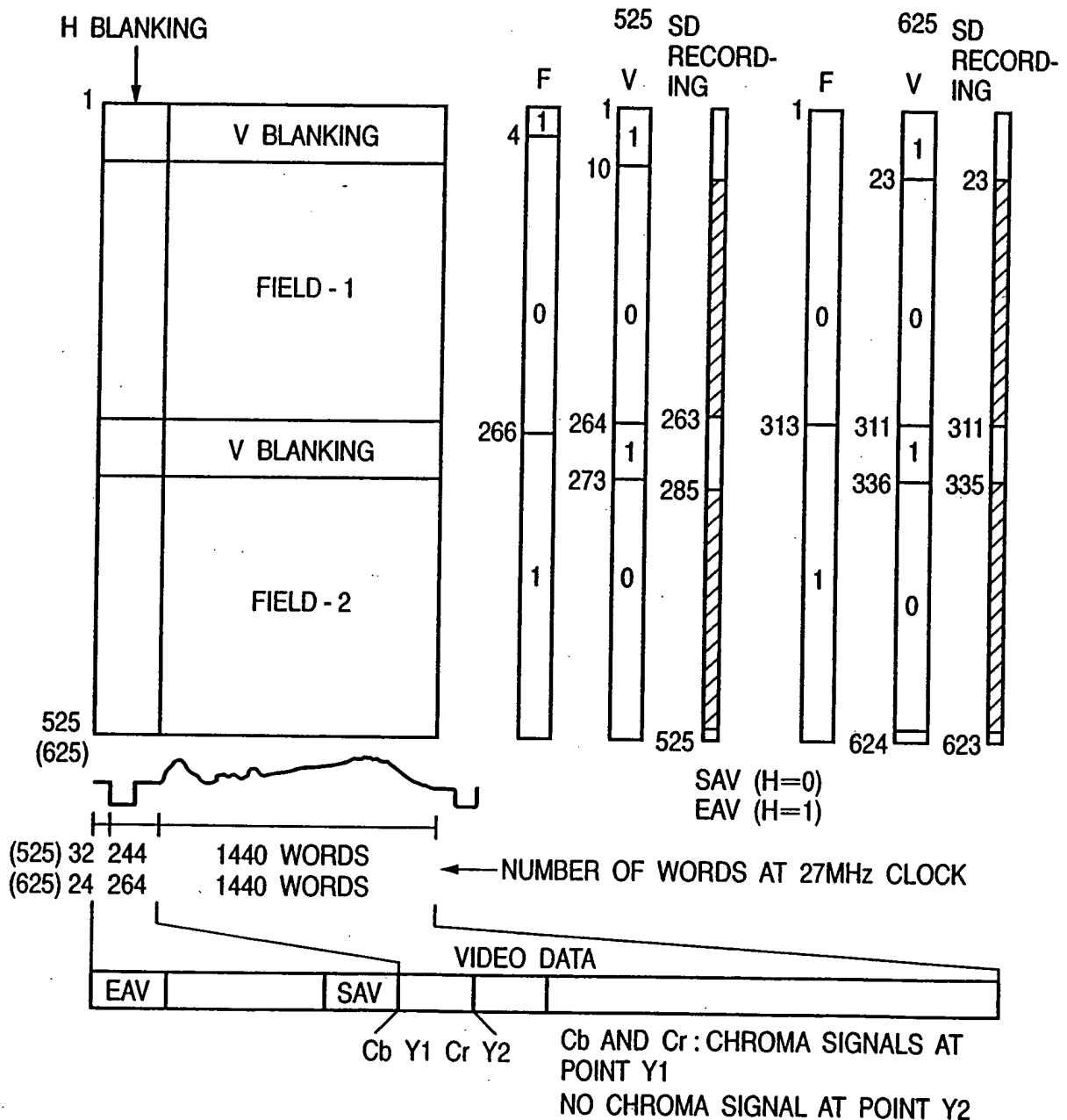


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PRIOR ART **FIG. 4**

EXPLANATORY VIEW OF RECORDING FORMAT CCIR Rec 601

4:2:2:1/F (IN CONFORMITY WITH CCIR Rec 601 / SMPTE 125M)



PRIOR ART

FIG. 5

EXPLANATORY VIEW OF RECORDING FORMAT CCIR Rec 601

CONTENTS OF EAV, SAV

	MSB	6	5	4	3	2	1	LSB	F	V	H	P3	P2	P1	P0
FIRST WORD	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
SECOND WORD	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1
THIRD WORD	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1
FOURTH WORD	1	F	V	H	P3	P2	P1	P0	1	0	1	1	0	1	0
									1	1	0	1	1	0	0
									1	1	1	0	0	0	1

00h AND ffh ARE NOT USED IN VIDEO DATA

10h (PEDESTAL LEVEL) IS USED IN OTHER POSITIONS THAN SAV AND EAV (BLANKING)

80h IS USED IN POSITIONS OF Cb AND Cr

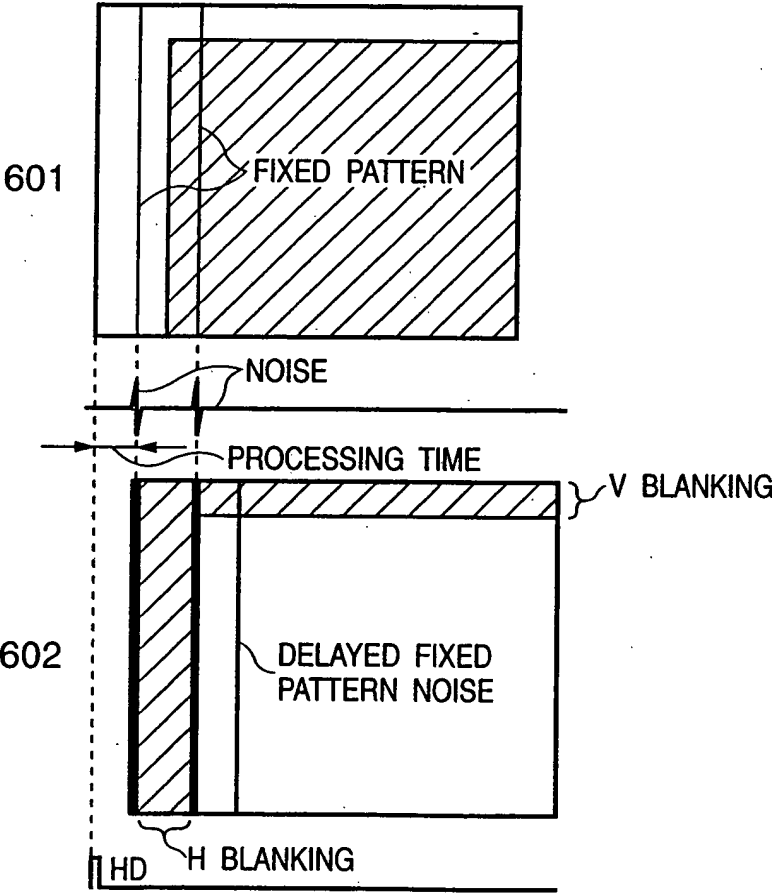
SAV AND EAV EXIST IN ALL LINES (ALSO IN V BLANKING)

PARITY IS ALWAYS ADDED ON TRANSMITTING SIDE, AND USED ARBITRARILY ON RECEIVING SIDE

PRIOR ART

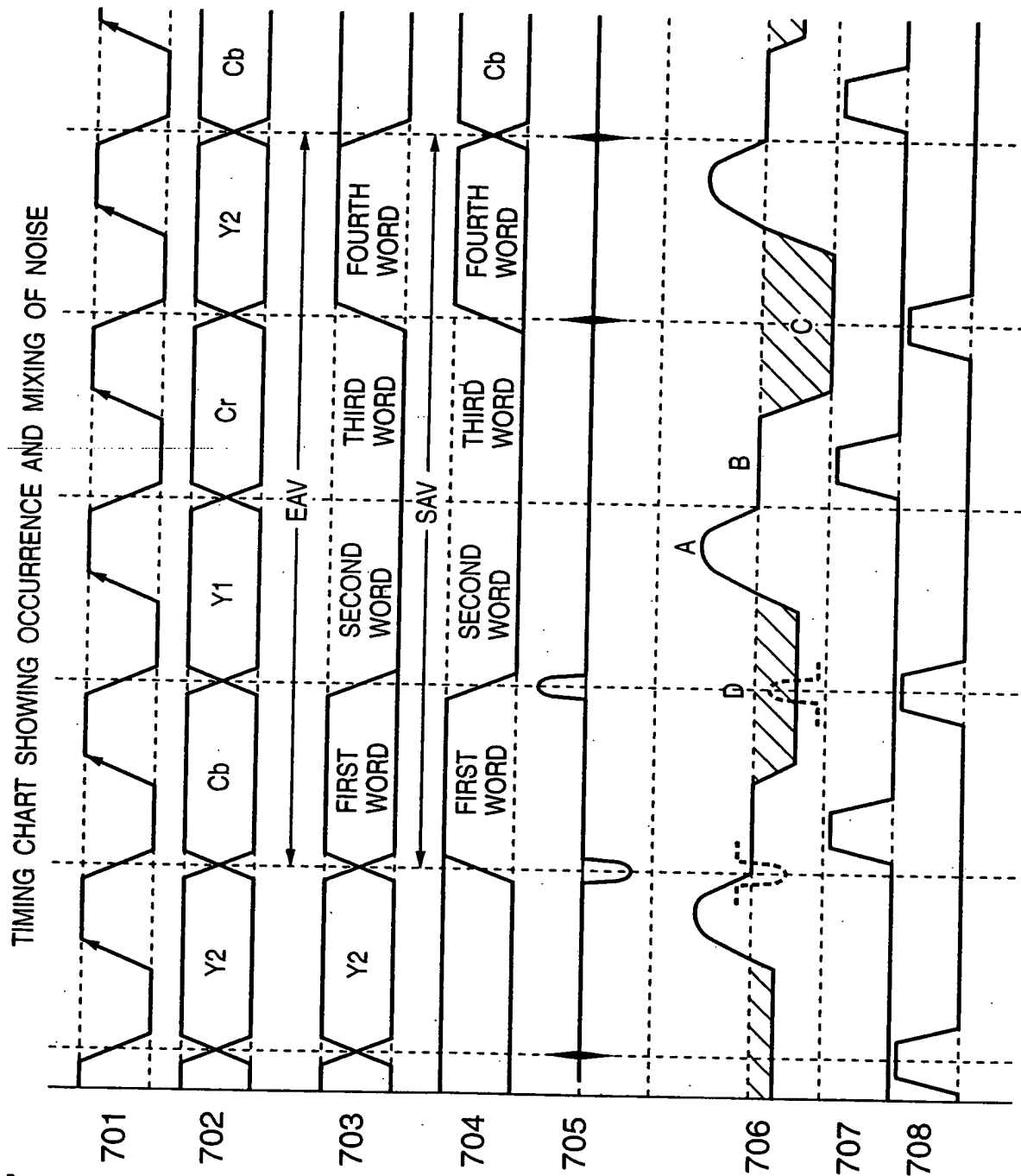
FIG. 6

SCHEMATIC DIAGRAM SHOWING NOISE OCCURRENCE
POSITION IN CONVENTIONAL ART



PRIOR ART

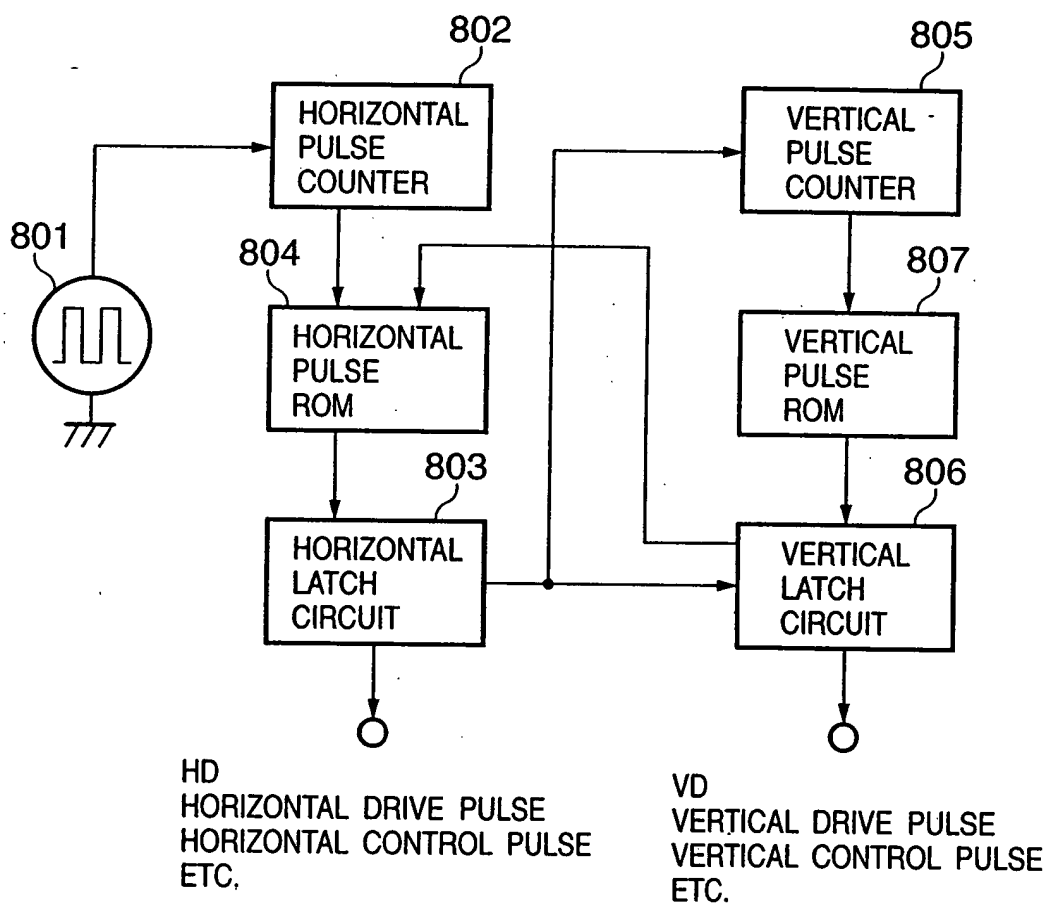
FIG. 7



PRIOR ART

FIG. 8

BLOCK DIAGRAM SHOWING CONSTRUCTION OF CIRCUIT TO GENERATE
SYNCHRONIZING SIGNALS AND CONTROL SIGNALS



PRIOR ART

FIG. 9

BLOCK DIAGRAM SHOWING ARRANGEMENT OF PROCESSING FINAL STAGE AND
PARALLEL BUS DRIVE CIRCUIT IN VTR SIGNAL PROCESSOR

